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Application Note

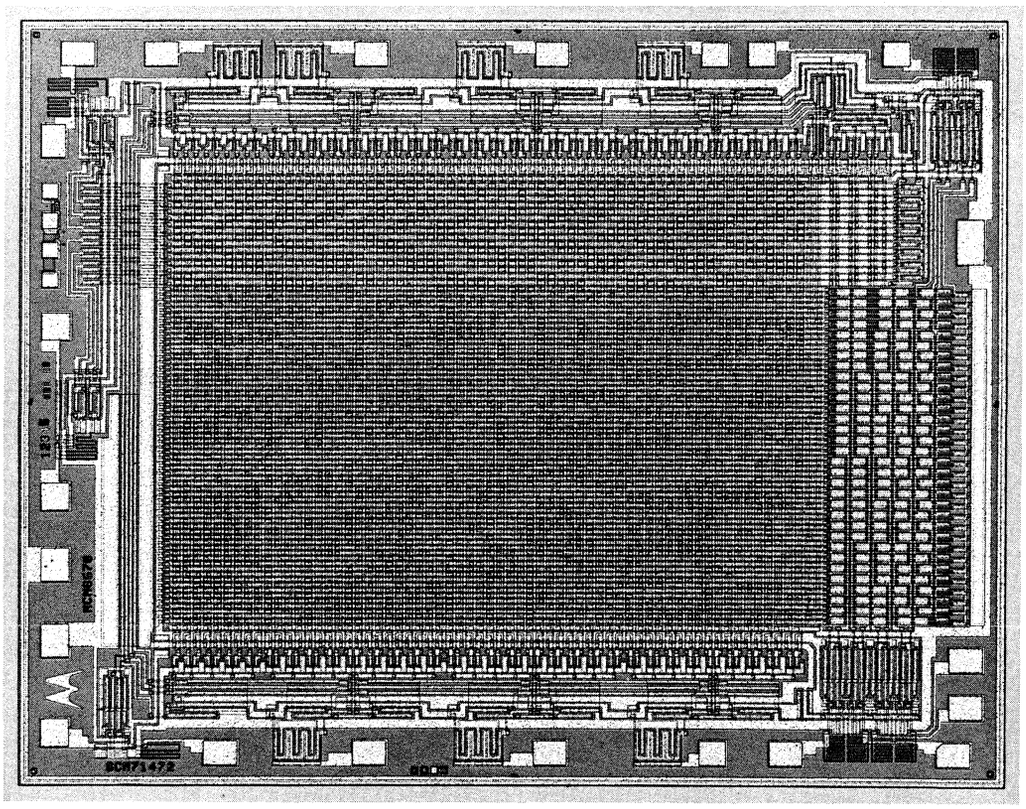
A CRT DISPLAY SYSTEM USING NMOS MEMORIES

Prepared by
Applications Engineering

New NMOS Memory devices used for both storage and character generation are demonstrated in a typical CRT display system. The 128-character system design features full TTL compatibility of the NMOS memories and design simplicity.

MOTOROLA *Semiconductor Products Inc.*

A CRT DISPLAY SYSTEM USING NMOS MEMORIES



The emerging NMOS semiconductor technology offers electronic equipment manufacturers improved circuit performance and density. Development of the NMOS process brings a new era of high-density memory technology, and it shows great promise for replacing core and other type memories. For CRT display manufacturers, however, NMOS technology is here today with the introduction of the MCM6571 8K Character Generator and the MC6545 quad 80-bit Shift Register. This paper describes a CRT display system using these devices.

BASIC CRT OPERATION

The basic elements of a display system is the CRT and the circuitry necessary to deflect and modulate the electron beam. The system must be capable of generating graphics and/or alphanumeric characters. The operation of most video display systems is similar to a TV set. The electron gun shoots a beam of electrons toward a screen coated with a light emitting phosphor. Wherever the beam strikes, a dot of light is emitted. The beam is deflected vertically and horizontally by either electrostatic or elec-

tromagnetic fields. The Z-axis grid can switch the electron beam on and off. By modulating the beam with the Z-axis grid, dots and line segments can be formed on the screen.

Due to the fact that the screen phosphor can hold the image for only a short time, the image must be constantly refreshed. The refresh rate is usually between 30 and 60 Hz. Because of the Z-axis modulation and the refresh requirement, two types of components are especially important to an alphanumeric CRT display: a character generator for modulating the Z-axis to form the character, and a storage device to retain the information to be refreshed on the screen.

CHARACTER FORMATION

The most popular type of character formation being used today is the dot matrix method. Figure 1(a) shows the dot matrix which must be generated at every character location to form the image. Any size dot matrix is possible, but 5 x 7 and 7 x 9 are the most popular configurations with the 7 x 9 offering clearer definition. Any character can be formed within the matrix by illuminating the proper dots (see Figure 1(b)).

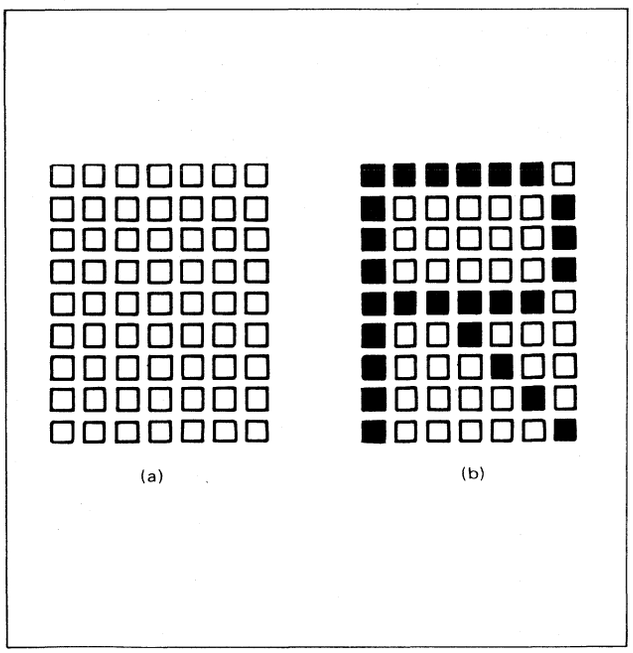


FIGURE 1

Systems using the dot matrix formation will usually generate a raster on the screen of the CRT. If a horizontal AC field is applied to the electron beam, it traces and retraces a line across the screen. If, at the same time, a vertical AC field of a lower frequency is applied and if the beam is shut off during retrace, many lines are generated, and a horizontal raster scan is formed (see Figure 2). Interchanging the frequencies generates a vertical scan. Dot matrices can be formed and separated at every character location by blanking the electronic beam in between matrices. The character location map shown in Figure 9 demonstrates this formation. The numbers indicating column and line location are explained later. As

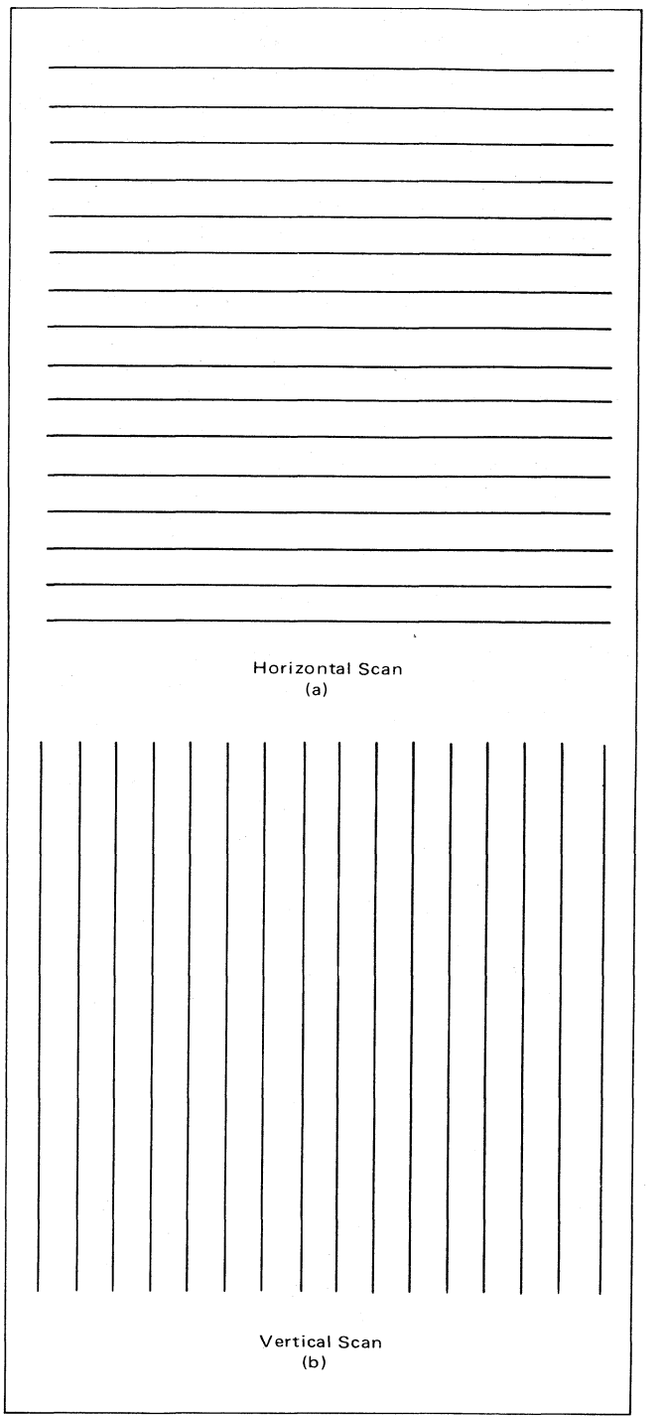


FIGURE 2

mentioned before, a character can be formed in each matrix by illuminating the proper dots.

The device that determines which dots are to be illuminated is called a character generator. Actually, it is a read-only memory containing a dot matrix pre-programmed for each character. Because of pin limitations, the entire dot matrix usually cannot be read out at one time. Instead, characters are read out a row or a column at a time. A row character generator would most efficiently be used with a horizontal scan and a column character generator, with a vertical scan display.

8K-BIT CHARACTER GENERATOR

NMOS technology has produced a new character generator with greater storage capability than the older PMOS devices. The MCM6570 is an 8192 bit, row character generator that can be mask programmed with any desired set of 128 characters. This device can be programmed in Japanese, Hebrew, or any special type of character or symbol format. It generates each character in a 7 x 9 matrix, and it is capable of automatically shifting descenders (such as g, j, p, q, and y). It is directly TTL compatible. This device can also interface directly with other NMOS devices and with Complementary MOS when using a +5 volt power supply.

A 7-bit character code (see Figure 3) is used to select any one of the 128 available characters. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected. As the row select inputs are sequentially addressed, the ROM will automatically place the 7 x 9 character in one of two pre-programmed positions on the 16 row matrix (see Figure 6), with the positions defined by the four row select inputs. Maximum access time is 500 ns; however, if a device is programmed with shifted characters, the access time can be reduced to 300 ns.

The MCM6571 is a pre-programmed version of the MCM6570 with a modified USASCII code input. It contains the upper and lower case English alphabet, commonly used lower case Greek letters, numbers 0 to 9 and various mathematical symbols and punctuation marks. In fact any type of specialized symbols can be generated. Figure 6 shows which row of the character matrix is generated for each of the possible row select inputs. When a descending character is selected, rows R14 thru R12 are automatically blanked. The next nine rows form the descending character matrix. Thus, while any one character is contained in a 7 x 9 matrix, a 7 x 12 matrix must be available on the CRT screen to contain both normal and descending characters. The MCM6571 uses a down count to display the rows of the character from top to bottom. The MCM6570 mask-programmable ROM allows a choice of either an up or a down count for this function.

The MCM6570 requires three power supplies: -3, +5, and +12 volts. In systems using only +5 volts, special requirements of -3 and +12 volts can be an inconvenience. Because the device requires only small amounts of current from these supplies, and charge pump techniques using +5 volt supply can be used. A supply shown in Figure 4 will generate the required -3 volts at less than 100μa. In Figure 5, a +12 supply is shown that will provide the 6 ma that typically is required from the 12V source.

STORAGE

As discussed earlier, the image on the CRT must be constantly refreshed; thus, a storage device is required to retain the information. Two types of storage devices can be used in this application: Random Access Memories and shift registers. RAM's offer the cost advantages resulting from high volume use and offer minimum access time when interfacing with a computer. Also, because of the random-access feature, no buffer storage is required. Shift registers are also low-cost devices offering simple editing functions; in particular, insertion operations.

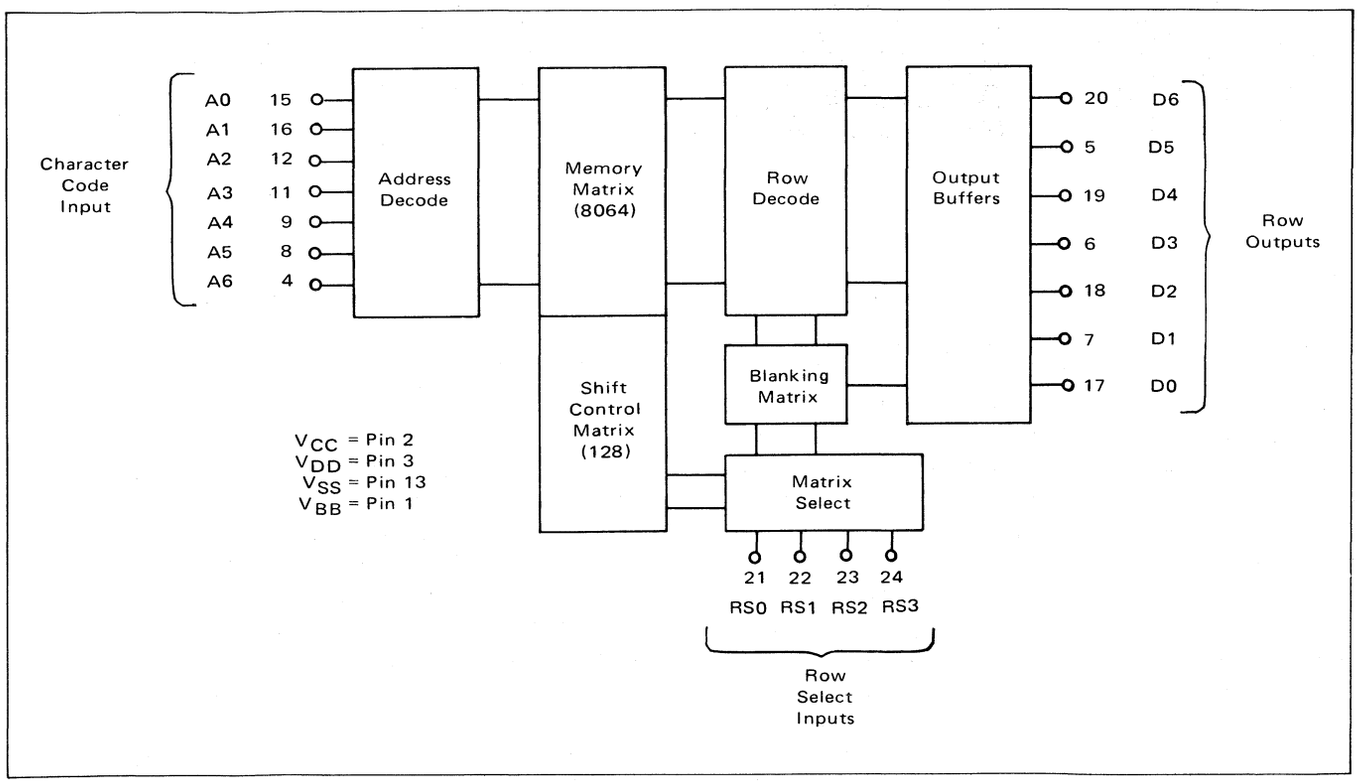


FIGURE 3

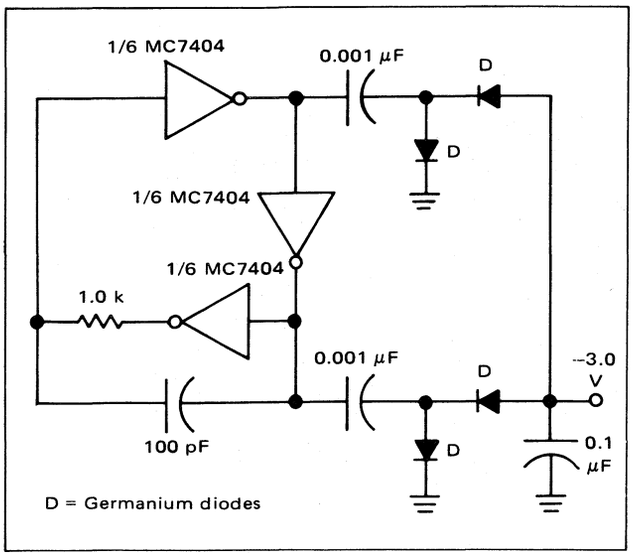


FIGURE 4 – – 3 VOLT POWER SUPPLY

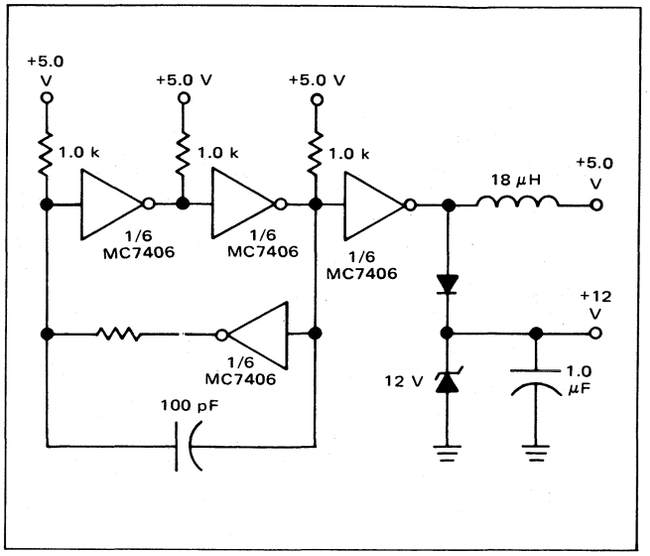


FIGURE 5 – +12 VOLT POWER SUPPLY

ROW SELECT
TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15

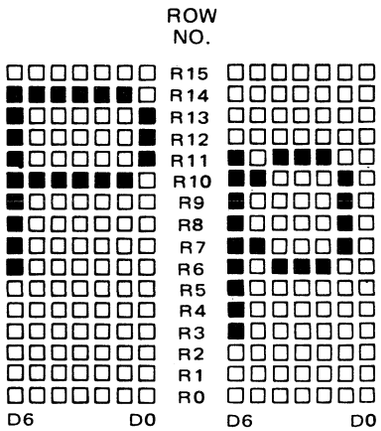


FIGURE 6

The necessity of a buffer register is an unattractive requirement of shift storage. Buffer storage is necessary because of the way the characters are written on the screen (see Figure 7). As the electron beam moves across the screen, each character code is applied in turn to the character generator and the first row of each character is read out. At the end of the row, the electron beam retraces and begins moving across the screen again. The same set of character codes must be presented to the character generator again so that the second row can be written. This procedure must be repeated until all nine rows have been written. With shift register storage, the information for a particular line would not be available after the first row was written, unless the information were shifted all the way around. If the shift register is large, system speed limitations would result. The buffer register can be eliminated, if small shift registers (storage capability of only one or two lines) are used in parallel. An ideal feature of these small shift registers would be 3-state outputs.

An excellent device for this application is the MC6545 Quad 80-bit shift register. It is an NMOS device and thus, is TTL compatible and also it will interface with other NMOS and with CMOS devices. The Quad 80 features internal recirculate logic, and a single clock with frequency capability of D.C. to 5 MHz. The shift register's static storage mode is when the clock logic level is "0".

THE SYSTEM

A CRT display system designed and built using the MCM6571 for character generation and the MC6545 for storage is shown in block form in Figure 8. It can display up to 640 characters (16 lines with 40

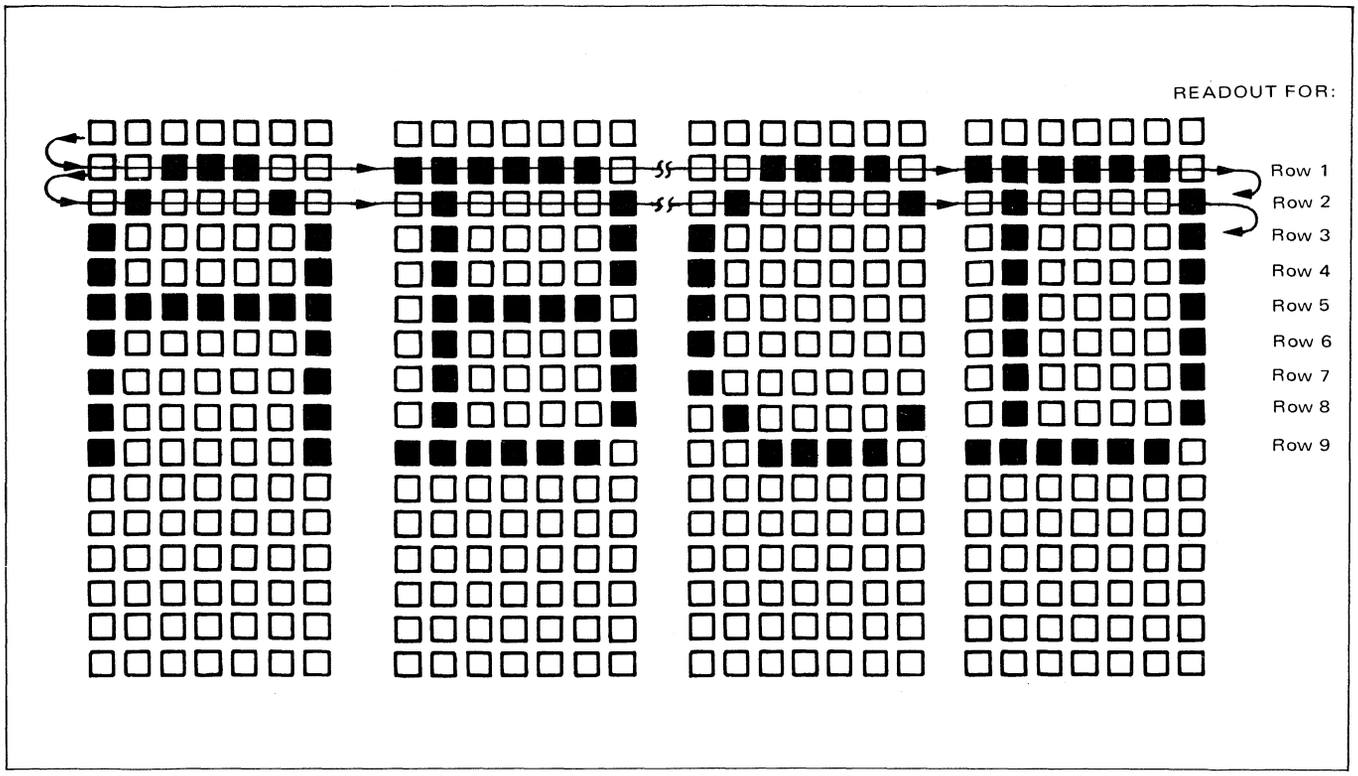


FIGURE 7

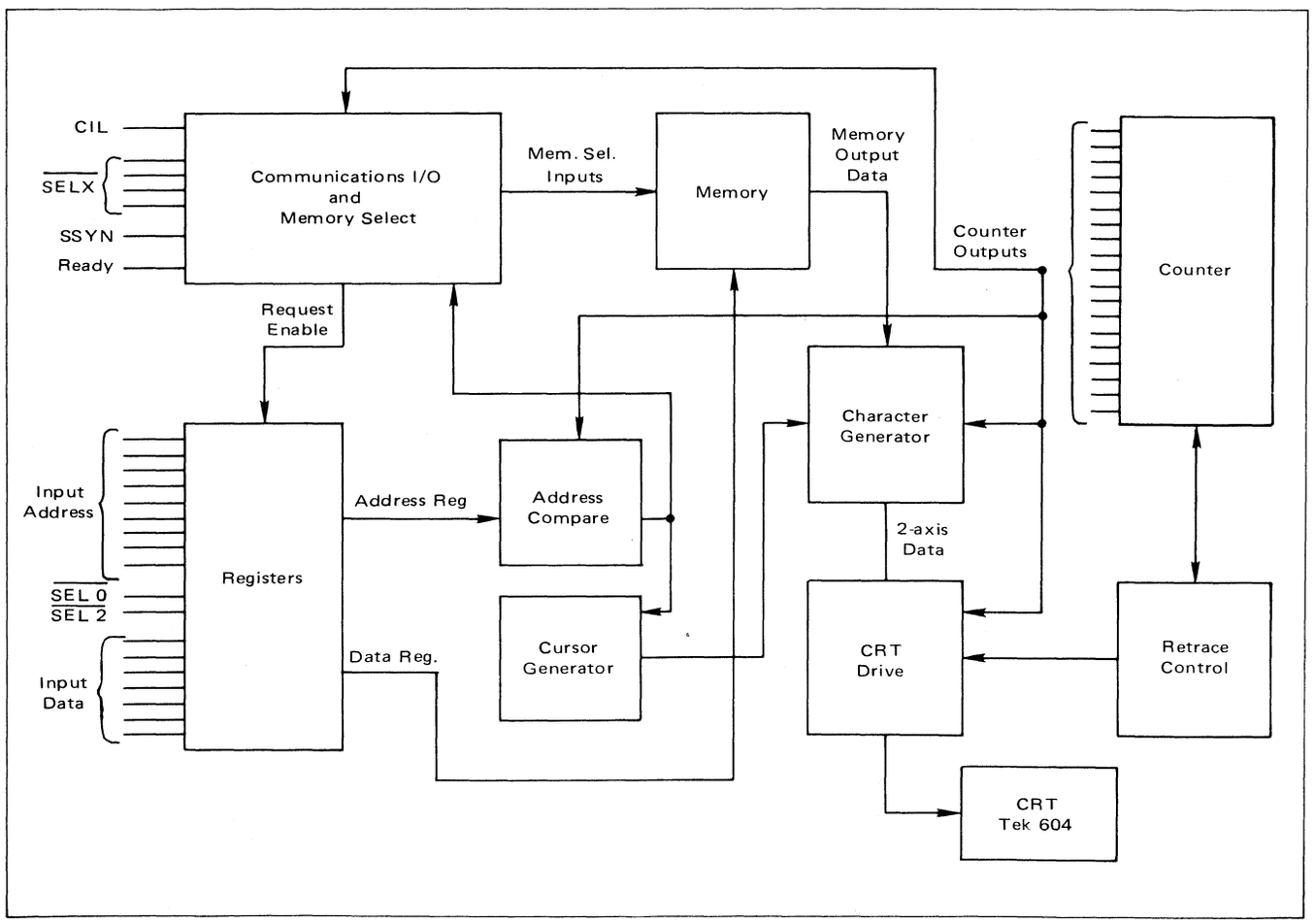


FIGURE 8

characters/line) and has a refresh rate of 60 Hz. The system is built on six circuit boards divided into the following function areas:

1) Counter and Retrace Control
2) Memory
3) Character Generation and CRT Drive
4) Input Address and Data, and Cursor Generation
5) Communications I/O and Memory Select
6) Power Supplies

The CRT display used is a Tektronix 604. It can be mounted in a standard 19" rack and the X, Y, and Z inputs can be driven by +5 and +12 volt supply circuitry. The other circuit blocks are mounted along side the 604. The counter is the central coordinator of the system, and it performs the following functions:

1. Associates a set of data bits in the shift registers with a character location on the screen
2. Signals the retrace control logic at the end of a row for horizontal retrace, and at the end of a frame for vertical retrace.
3. Provides timing signals for;
   a. Serializing the parallel data from the character generator onto the Z-axis.
   b. Initiating a Read or Write cycle requested from the computer.
   c. Erasing the screen.
   d. Entering data in the output data register.
   e. Clocking the shift register.
4. Selects the row of each character being brought out of the character generator.

Retrace control drives the logic for the X and Y amplifier inputs of the display unit and signals the Z-axis to turn off the electron beam during retrace. Memory stores the character code for each character location on the screen (even if it is a blank). Data from the memory drives the character generator which provides the dot matrix, one row at a time. This parallel data is converted and applied serially to the Z-axis. Communications input/output section accepts Read and Write requests from the computer, and enables the address and data bits into the Registers. It disables the recirculate input on the shift register when a write is required. Address Compare checks for equality between the data in the input address register and the counter address. When this equality is detected, one of several things can happen:

a. If the Write Request flip-flop has been set, Address Compare begins a Write cycle.

b. If the Read Request flip-flop has been set, Address Compare enables the data at this location into the Output Data Register.

c. In any case, Address Compare enables the cursor. If no equality is detected during a frame, and if there has been no computer request; the address in the Address Register is illegal and the screen is erased. Figure 9 shows the address map. The Cursor block generates a blinking cursor in row 2 (see Figure 6) of the character location in the Address Register.

COUNTER AND RETRACE CONTROL

A logic diagram of this board is shown in Figure 10. The counter is driven from an oscillator formed from two MC8602 one-shots in a single package. (1). The desirability of this type of oscillator will be discussed later in the memory section. The operating frequency is 5.0 MHz for a refresh rate of precisely 60 Hz. Because the counter is synchronous, the oscillator drives all the devices in the chain.

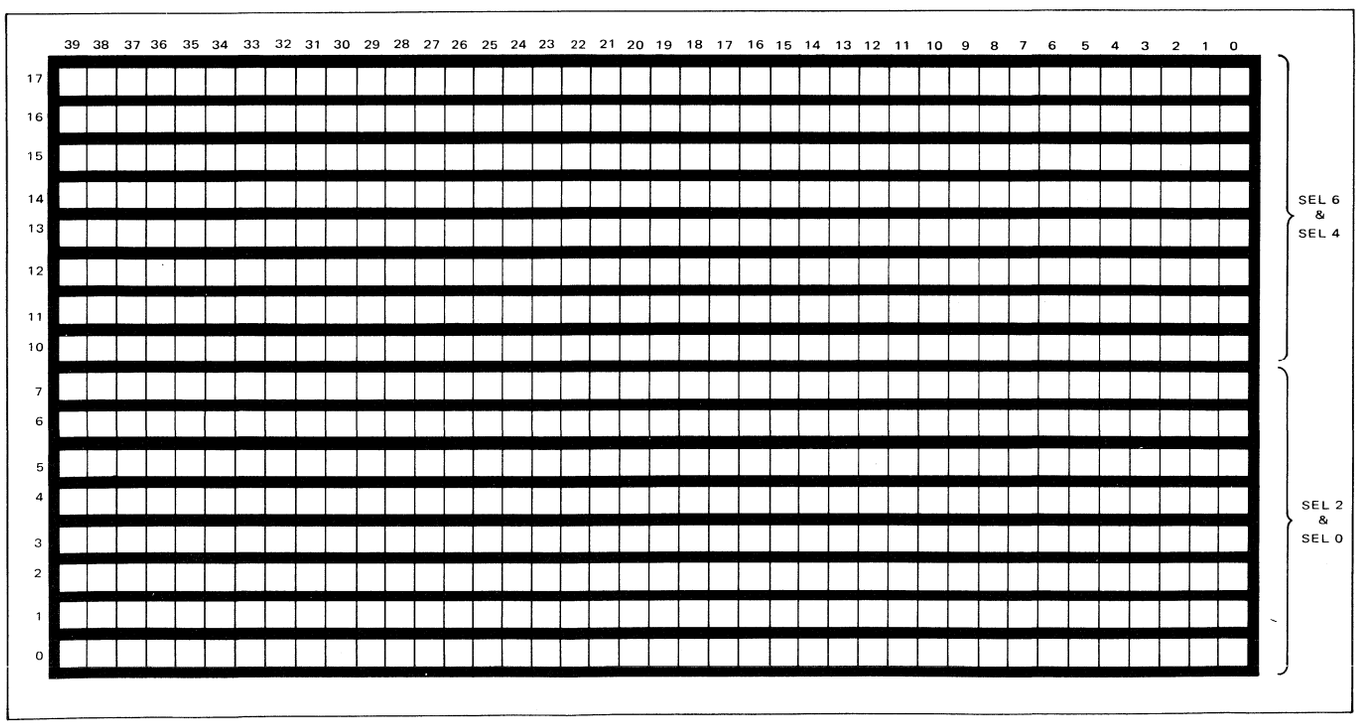


FIGURE 9

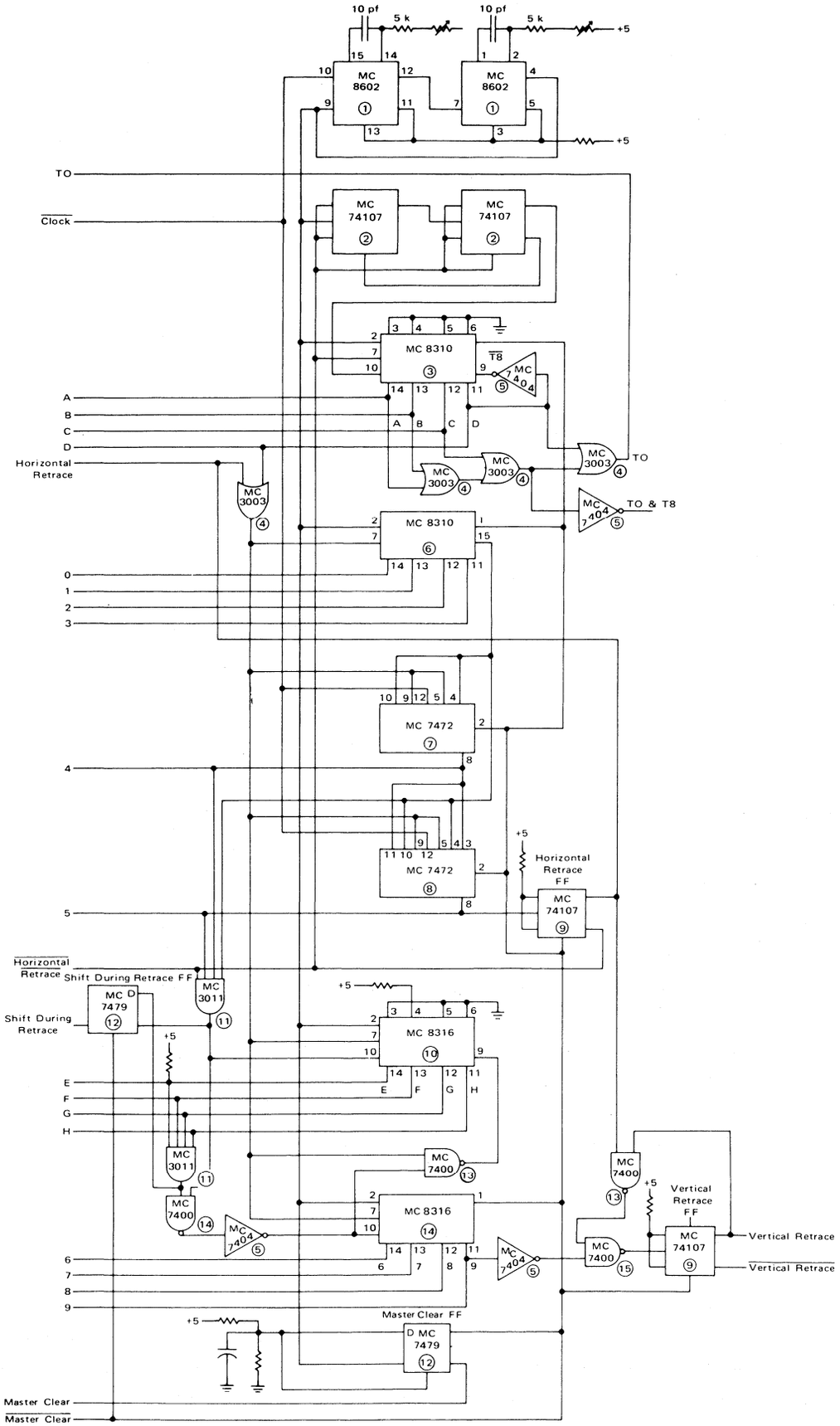

10 pf
5 k
10 pf
5 k
+5
MC 8602
MC 8602
+5
TO
Clock
MC 74107
MC 74107
MC 8310
T8
MC 7404
A
B
C
D
Horizontal Retrace
MC 3003
MC 3003
MC 3003
MC 3003
TO
MC 7404
TO & T8
MC 8310
0
1
2
3
MC 7472
4
MC 7472
+5
Horizontal Retrace FF
MC 74107
5
Horizontal Retrace
Shift During Retrace FF
MC 3011
MC D 7479
Shift During Retrace
+5
MC 8316
E
F
G
H
MC 3011
MC 7400
MC 7400
MC 7404
MC 8316
MC 7400
+5
Vertical Retrace FF
MC 74107
Vertical Retrace
Vertical Retrace
MC 7400
MC 7404
6
7
8
9
Master Clear FF
+5
D MC 7479
Master Clear
Master Clear

FIGURE 10

The first stage of the counter is an MC8310 (3) which has been connected to count decimally from 0 to 8. The dot matrix columns 1 through 7 are being written when the count in this register is 1 through 7. During counts 0 and 8, the Z-axis is blanked to form a space between horizontally adjacent characters. (4) and (5) are used to generate the time "T0", "$\overline{T8}$", and "T0 + (or) T8". In addition to the clock input, (3) is enabled by (2) and (9). The function of (2) is to delay the beginning of trace by two clock pulses. The necessity for this delay will be discussed later. Circuit (9) is the horizontal retrace flip-flop which enables this MC8310 (3) during the trace operation and disables it during retrace (see Figure 11). As mentioned earlier in order to write one line of characters the codes must be presented to the character generator once for each row of the dot matrix. In addition, the shift register must be shifted completely around between the beginning of one trace and the start of the next. The shift register is 80-bits long and the number of characters in a line is 40. Thus, the other 40 must be shifted during retrace; as will be explained later, this second set of 40 character codes is for the line following the first set of 40. Since the time for trace is nine times as long as the time for retrace, the second 40 bits must be shifted faster. To obtain this fast shift, (9) disables (3), effectively taking it out of the counter, and enables (6), which is the second stage of the counter, to be driven at the clock frequency. During trace, (6) is driven at the clock frequency divided by 9.

An MC8310 (6), and two MC7472's, (7) and (8), form a 6-bit counter stage to count decimally from 0 to 39. The count in this stage determines the horizontal character position on the screen. During retrace, this stage goes through its full count at the clock frequency and during trace, at the clock frequency divided by 9. At the end of each count the Horizontal Retrace flip-flop, (9), is toggled. Figure 12 shows the necessity of (2). During retrace the character codes are being shifted at a rate of

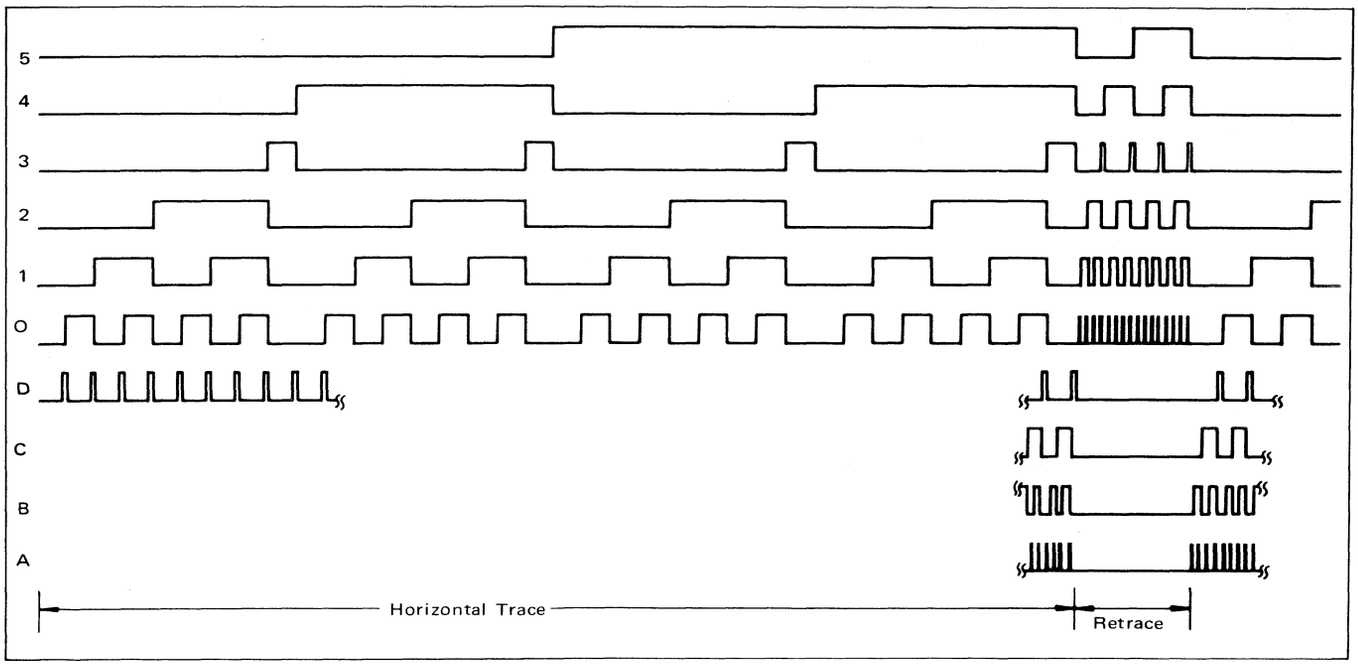


FIGURE 11

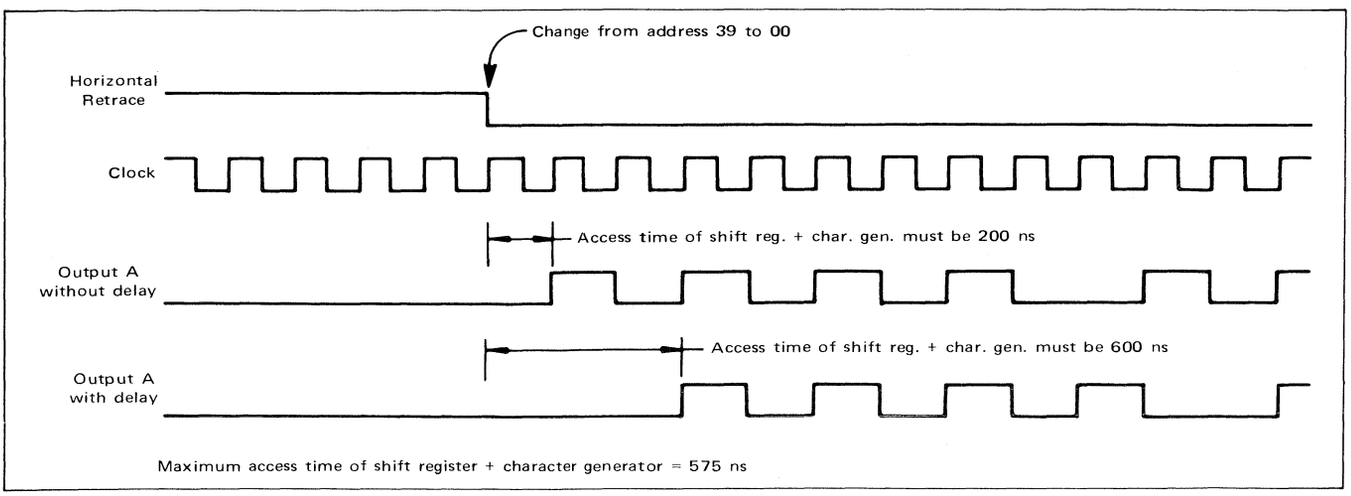


FIGURE 12

5.0 MHz; the maximum access time for the character generator and shift register is 500 + 75 = 575-ns. If there were no delay after the completion of retrace, the output for character location 0 would be required after 200-ns. By inserting a delay of two clock pulses this timing is increased to 600-ns.

The next stage of the counter is an MC8316, (10), a 4-bit counter which counts octally 2 to 16 (see Figure 10). The count in this device determines which dot matrix row is to be read out of the character generator. It is enabled when the count in the previous stage is completed and just before the Horizontal Retrace flip-flop (9) is set. This function is controlled by an MC3011 (11), that also serves as clock for the Shift During Retrace flip-flop, an MC7479 (12). As mentioned before, the data must normally be shifted during retrace. When one line of characters has just been completed and another is to begin, the shift must be inhibited. Thus, the Shift During Retrace flip-flop is clocked as each row is completed. If additional rows in the character line must still be written, the D input will be at logic "0" and the shift will be enabled. If the completion of the row is also the completion of the line (the count in (10) = 16), the D input will be a "1" and the flip-flop set, and this will inhibit Shift During Retrance. An MC3011, (11) decodes the count in (10) and drives the D input of (12).

The outputs of both gates of the MC3011 (11) are "ANDED" to form an enable for the last counter stage, MC8316 (14). It counts octally from 0 to 17. The count in this device determines the vertical character position or character line. At the end of the last count, the vertical retrace flip-flop is set. A vertical retrace takes the same amount of time as a horizontal retrace thus the Vertical Retrace flip-flop is reset by the Horizontal Retrace flip-flop. The Master Clear flip-flop initializes the system when power is first applied.

MEMORY SELECT

The Memory Select section (see Figure 13) forms the Shift Register Clock, and enables the Write and Output Enable inputs of the selected shift registers (MC6545). An MC4038 decodes the 3 highest order bits of the counter to generate an Output Enable. A set of MC3006 logic gates generates a Write Enable for the selected pair of shift registers when a Write cycle is being executed, and an Address Compare indicates that the desired location has been reached.

When the Horizontal Retrace flip-flop is reset, an MC3031 uses output C of the counter to clock data out of the shift registers. When the Horizontal Retrace flip-flop is set, and a Shift During Retrace is required, the counter clock is enabled by the MC3031 to form the Shift Register Clock. The MC3031 output goes to an MC7440 high fan-out driver which in turn drives the clock inputs of all 16 shift registers.

At this point, the desirability of the double one-shot oscillator for the counter clock becomes apparent. The Shift Register Clock is required to be in the high state for at least 90-ns and in the low state for at least-90ns. Since the counter clock runs at 5.0 MHz (200-ns), a duty cycle close to 50% at the shift register clock input is required. The counter clock pulses go through an MC3031 and an MC7440 before reaching the shift register clock input; thus, some skew in the positive and negative propagation times may occur. To compensate for this skew, the pulse widths of the two one-shots can be adjusted as required.

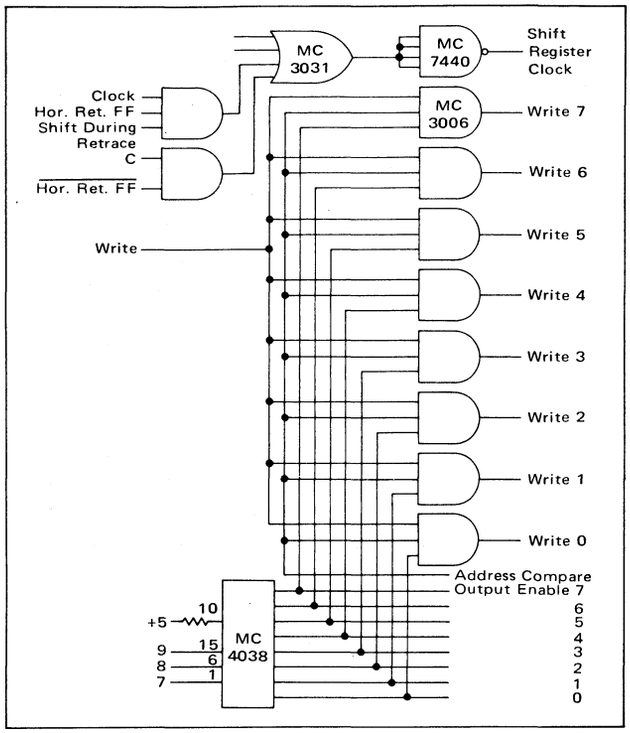


FIGURE 13

MEMORY

The Memory section (see Figure 14) consists of sixteen MC6545 shift registers arranged in pairs and 16 MC8T26 three-state buffers. Each pair holds 80 seven-bit character codes for two lines of display. The MC8T26 buffers are required so that only one pair of shift registers is being accessed at a time.

CHARACTER GENERATION

The output data from the shift registers goes to the Character Generation section (see Figure 15). If the system is in a Read cycle, the data is enabled into the Output Data Register made up of two MC7475's. In any case, the data goes to the character generator as does the row select count from the counter. The specified row for the character is read out of the character generator and stored in the Output Row Register at T0 + T8 time. The Output Row Register is applied to an 8-channel data selector, MC8312. This device selects each row input to be enabled to the single output according to the input count. This is supplied by the three lowest order bits of the counter. Thus, the parallel data is converted to serial data. At T0 and T8 times, the grounded input pin is enabled.

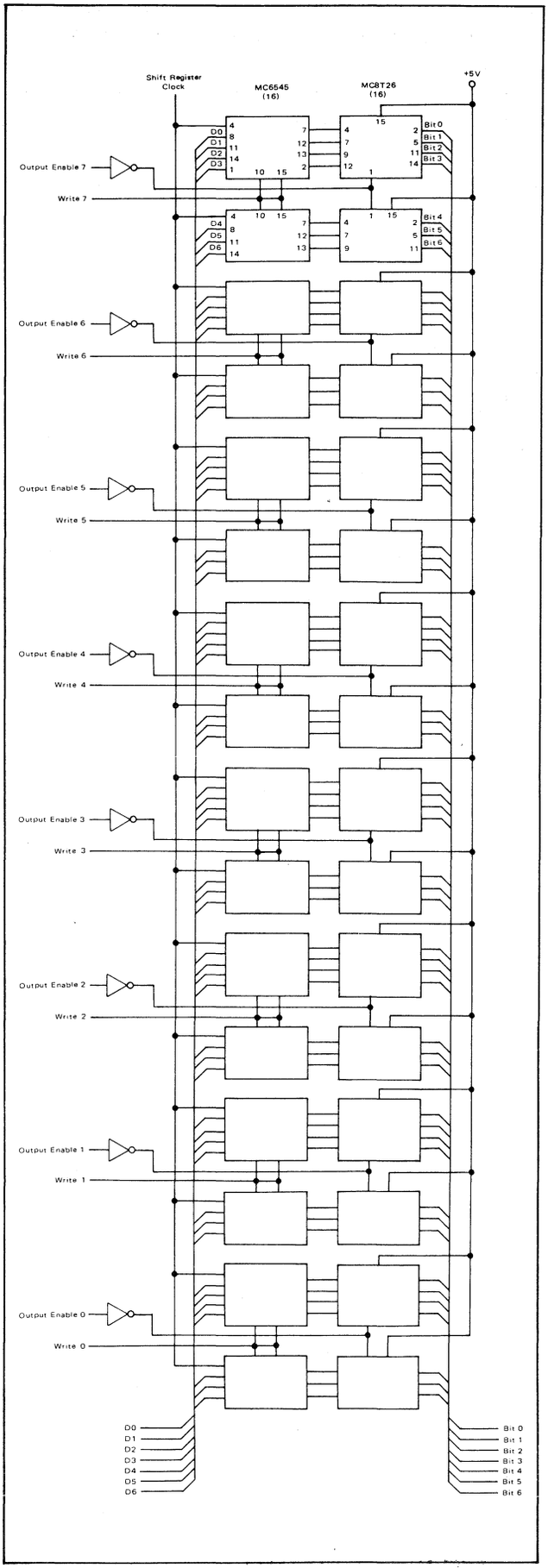


FIGURE 14

The MC8312 also has an enable input which is driven by the cursor generator to be described later.

The output of the MC8312 goes to the Z-axis driver which consists of 3 collector-or'ed MC7417's driving an output transistor. The Z-axis driver output goes to "0" during vertical and horizontal retrace and whenever the data input from the MC8312 is "0".

CRT DRIVE

The output drivers for the X and Y axes are shown in Figure 16. Each is driven by a cross-coupled gate/flip-flop, MC7400, which is, in turn, set and reset by two pulses tapped from the outputs of an MC7442 and MC4007. During retrace, these devices generate a series of timing pulses from the same counter bits that determine horizontal character location. Thus, retrace time can begin a short time after blanking begins, and it can end a short time before blanking ends. This method eliminates any distortion that might result from characters being displayed in the non-linear area of the raster edges.

COMMUNICATION I/O

The read/write logic is designed for use with a 16-bit bus-oriented minicomputer. The display system uses four addresses on the bus. A bus interface card generates four signals, $\overline{SEL0}$, $\overline{SEL2}$, $\overline{SEL4}$, and $\overline{SEL6}$, to indicate when these four addresses are selected. A control signal, C1L, indicates whether a bus-read or a bus-write cycle is being executed by the external control minicomputer. In order to respond to the minicomputer, the display system must generate two signals: 1) Ready, to indicate whether or not the system is busy doing an operation, and 2) SSYN, to indicate that a bus cycle is complete.

The four possible types of operations have been assigned as follows:

1) A bus write using either $\overline{SEL2}$ or $\overline{SEL6}$ is for writing data into the refresh memory. $\overline{SEL2}$ is for the bottom 8 lines of the display and $\overline{SEL6}$, the top 8 lines.

2) A bus write using either $\overline{SEL0}$ or $\overline{SEL4}$ is for specifying which location is to be read. $\overline{SEL0}$ indicates the bottom 8 lines of the display and $\overline{SEL4}$, the top 8 lines.

3) A bus read using either $\overline{SEL2}$ or $\overline{SEL6}$ is for determining the status of the Ready signal.

4) A bus read using either $\overline{SEL0}$ or $\overline{SEL4}$ is for retrieving the data requested in 2). For these operations, the 16-bit word of the minicomputer is divided into two sections. The seven least significant bits specify the character code, and the remaining nine specify the address.

The communications I/O logic is shown in Figure 17. A write operation is executed in the following manner (see Figure 18(a)):

1) Address and data are applied to the input lines of the CRT display system (Input Address and Data, and Cursor Generation are discussed in a later section). At the same time, C1L input goes to zero which enables the OR gate inputs to the Read and Write Request flip-flops.

2) A minimum of 150-ns later, $\overline{SEL2}$ or $\overline{SEL6}$ goes to zero which sets the Write Request flip-flop. In turn, it sets the SSYN flip-flop. Ready goes to zero, and the input address and data are enabled into the Registers.

3) The SSYN is transmitted back to the minicomputer which waits 75-ns and then changes $\overline{SELX}$ back to a one.

4) The SSYN flip-flop is reset and the SSYN signal goes to a zero.

5) When the Address Compare signal goes to a "1", indicating that the address register and the counter

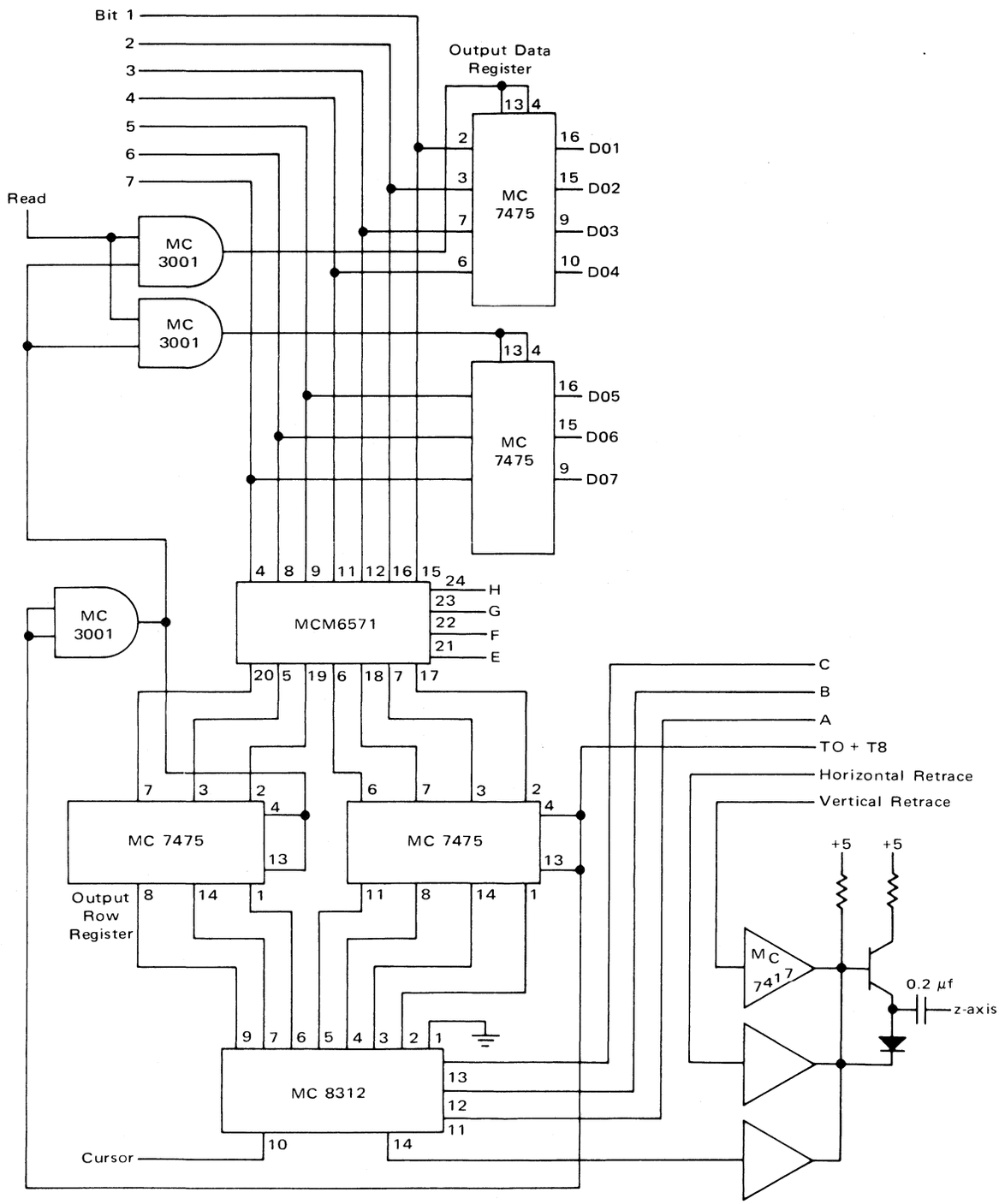


FIGURE 15

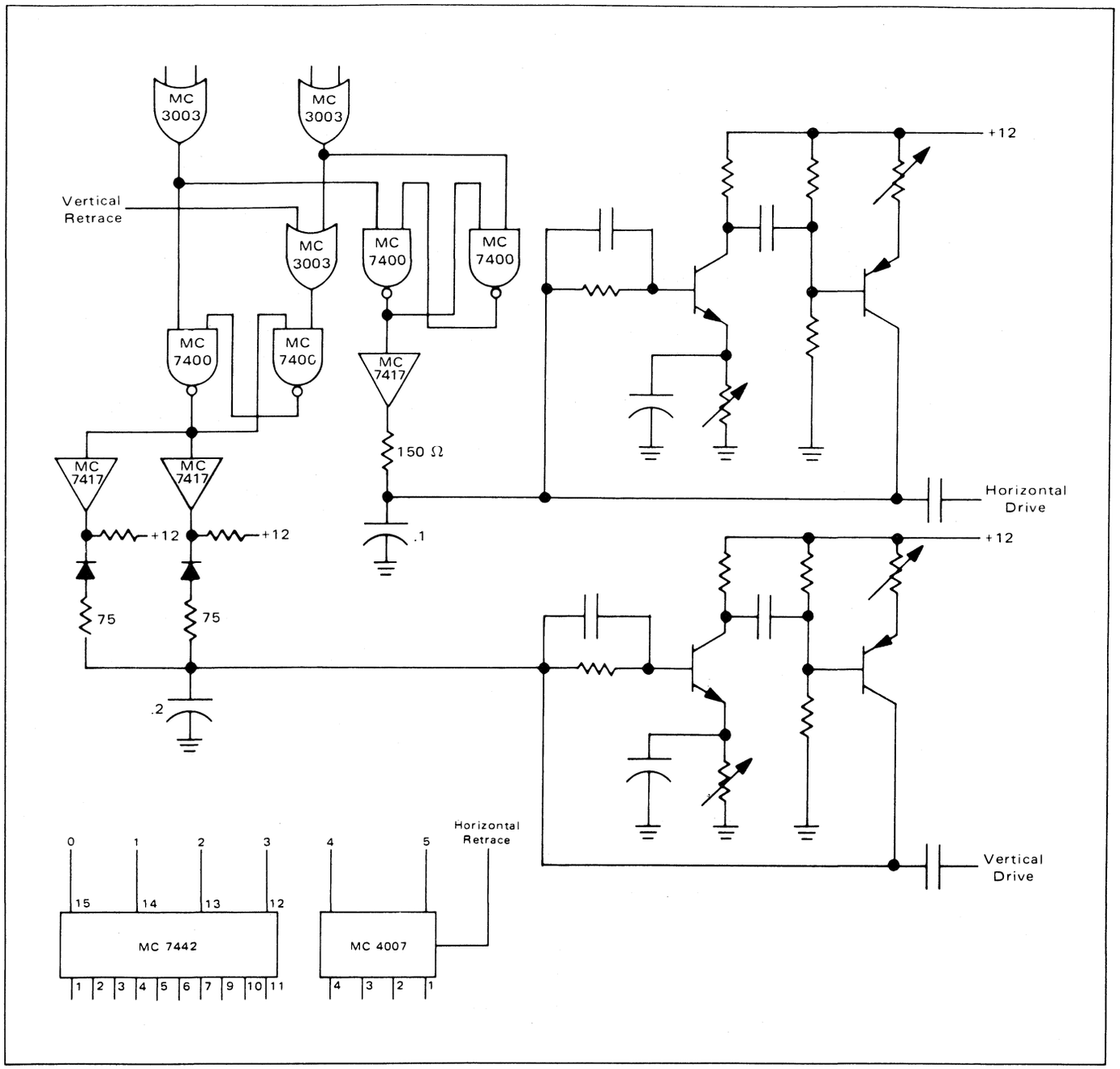


FIGURE 16

contain the same address, the Write Request is clocked into the Write flip-flop. This flip-flop enables the necessary logic to write the new data into memory. The Write flip-flop is set directly when an erase is being executed.

6) At the next T8 to T0 times respectively, the Write Request and Write flip-flops are reset and Ready goes to a "1". The system can now accept a new request.

A read operation (for specifying the location to be read) is done in a similar manner except the $\overline{\text{SEL0}}$ or $\overline{\text{SEL4}}$ are used.

To transfer data from the Output Data Register (see Figure 15) to the minicomputer or to check the status of the CRT system, the following sequence occurs (see Figure 18(b)):

1. C1L goes to a one.
2. A minimum of 150-ns later, one of the $\overline{\text{SELX}}$ signals goes to a zero.
3. The SSYN signal goes to a one for at least 75-ns.
4. The $\overline{\text{SELX}}$ signal returns to a one and SSYN goes to a zero.

INPUT ADDRESS AND DATA

The Address Register consists of two MC4015's and a MC7479 (see Figure 19). The input address is enabled into the register when the Read Request or Write Request flip-flop is set. The input to bit 9 of the Address Register is dependent on the $\overline{\text{SELX}}$ input. If $\overline{\text{SEL0}}$ or $\overline{\text{SEL2}}$ is used, a zero is entered into bit 9 which means the bottom 8 lines of the display will be accessed. If $\overline{\text{SEL4}}$ or $\overline{\text{SEL6}}$ is

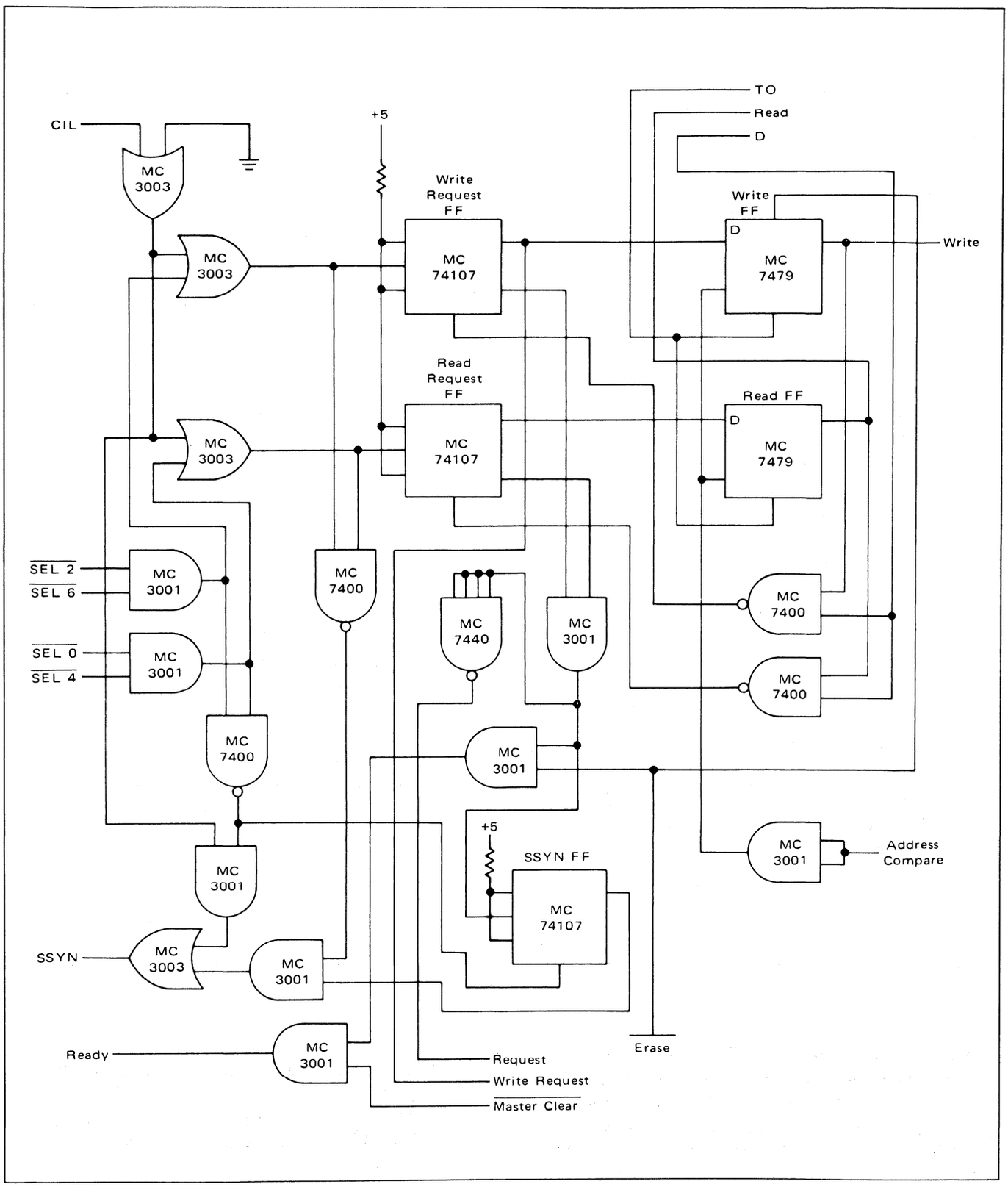


FIGURE 17

used, a one is entered into bit 9 and the top 8 lines will be accessed.

Ten MC8242 exclusive NOR gates are constantly comparing the input and counter addresses. They are open collector output devices; therefore, when they all indicate a compare, the output goes to a "1". The Address Compare flip-flop is set at the first positive edge of the B output of the counter. If a read or a write has been requested, it can be done at this time. Also the Address Compare flip-flop enables the cursor row compare logic and inhibits an Erase.

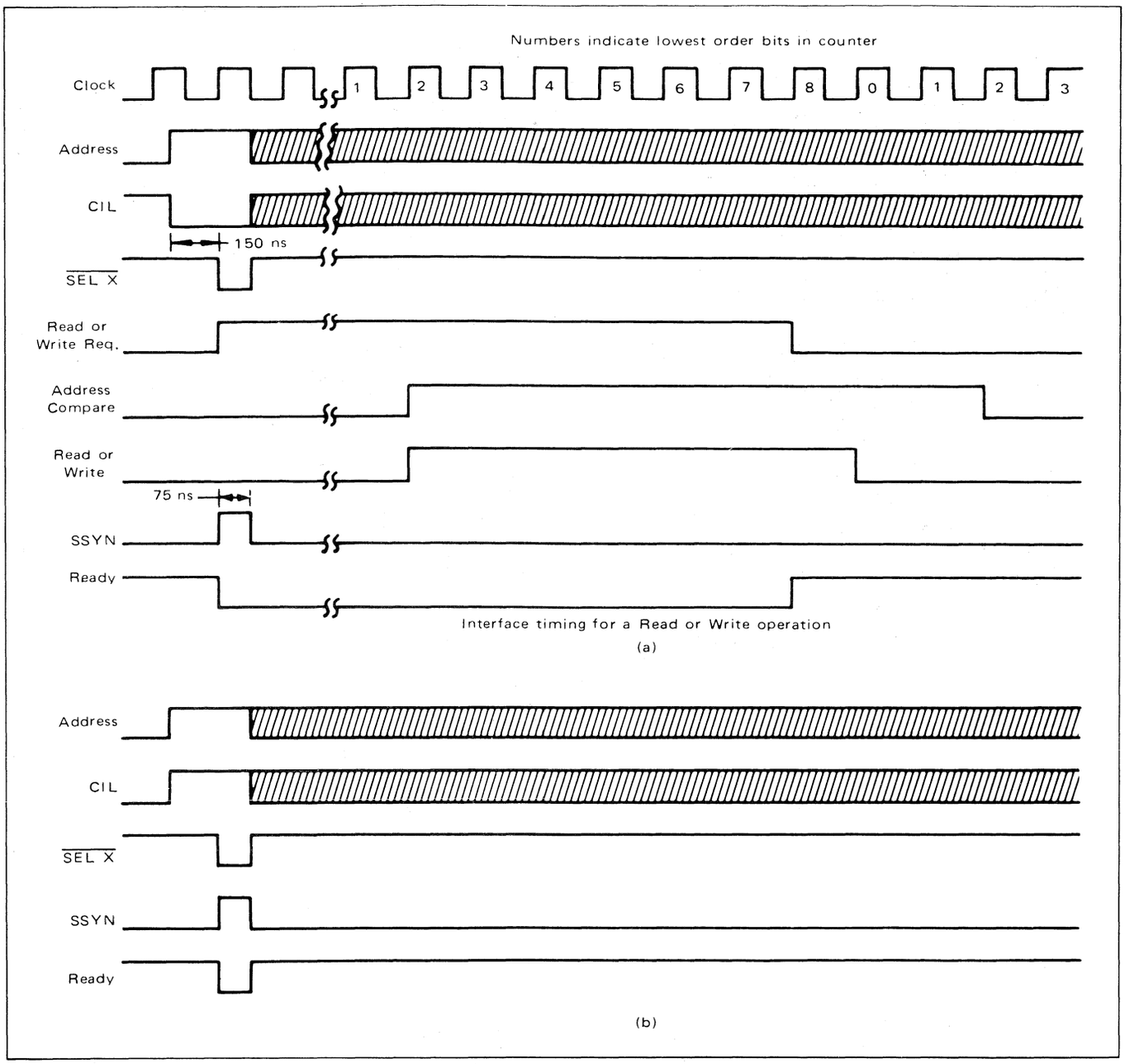


FIGURE 18

When Address Compare or a Read or Write Request goes from "0" to "1", the Erase Inhibit flip-flop is set. After each frame is written, the $\bar{Q}$ side of the Erase Inhibit flip-flop is clocked into the Erase flip-flop. As long as the latter stays reset, nothing happens. An illegal address can be entered into the Address Register however (an illegal address would be when the 4 lowest order bits of the Address Register contain a decimal number between 10 and 16). Since the counter does not duplicate the illegal address, the Address Compare flip-flop and, consequently, the Erase Inhibit flip-flop do not switch. At the end of the frame, then, the Erase flip-flop is set.

Setting the Erase flip-flop forces:

1. The input data to the shift registers to the character code for a blank.
2. The Address and Input Data Registers to all 0's.
3. The Erase Inhibit, Address Compare, and Write flip-flop's set.

This clears the screen of all data and moves the cursor location to address 0.

CURSOR GENERATION

The cursor is written at the location in the Address Register. It is written in row 2 of the dot matrix (see Figure 6). Four MC7405's are collector OR'ed (see Figure 20) to output a "1" each time that row select 2 and address compare exist at the same time. An MC7490 then divides the frequency of this output by five to make the cursor blink. The output of the MC7405's and the MC7490 are "ANDED" and, as mentioned earlier, the signal is used to drive the enable input of the parallel to serial converter for the Z-axis, MC8312.

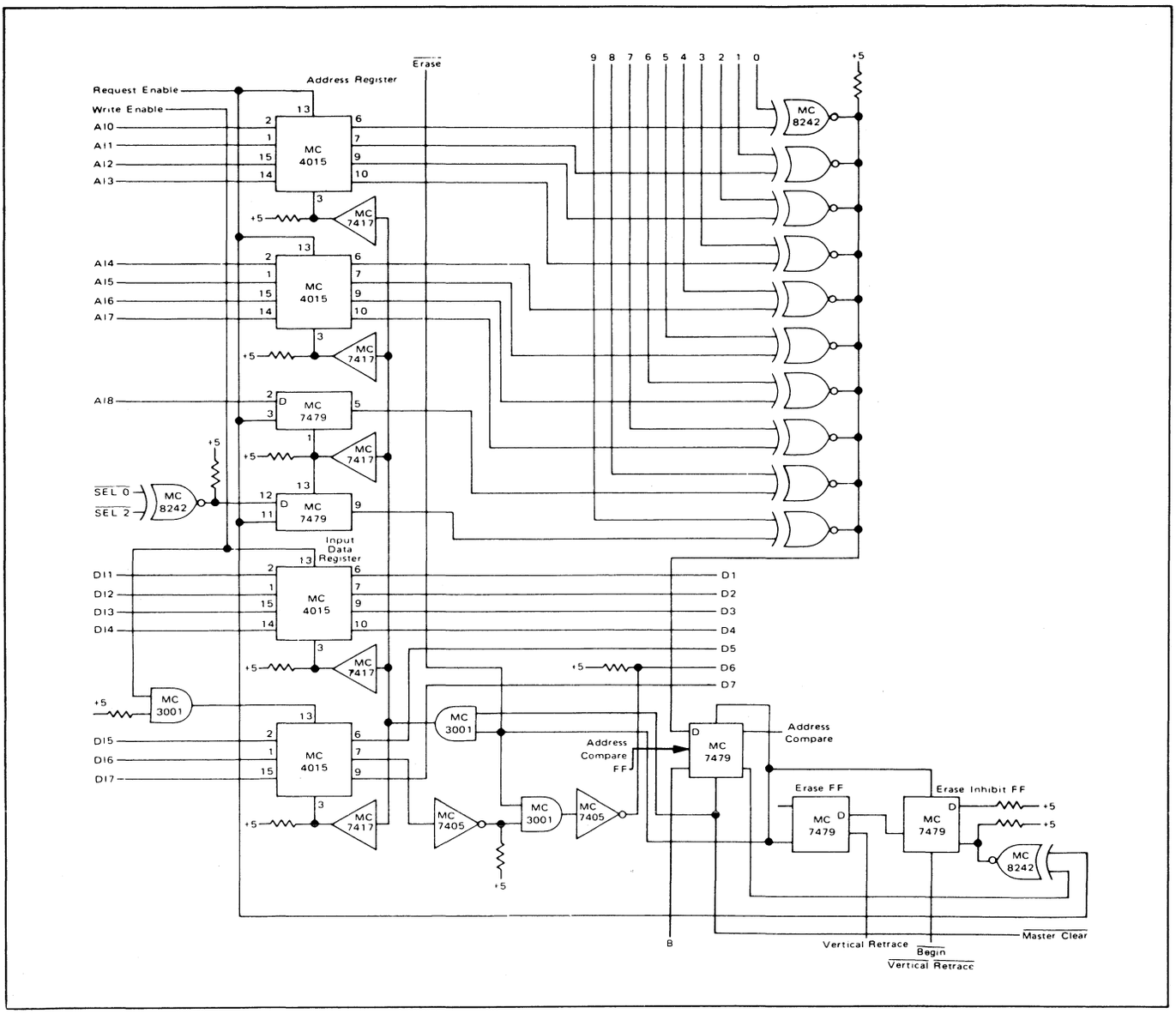


FIGURE 19

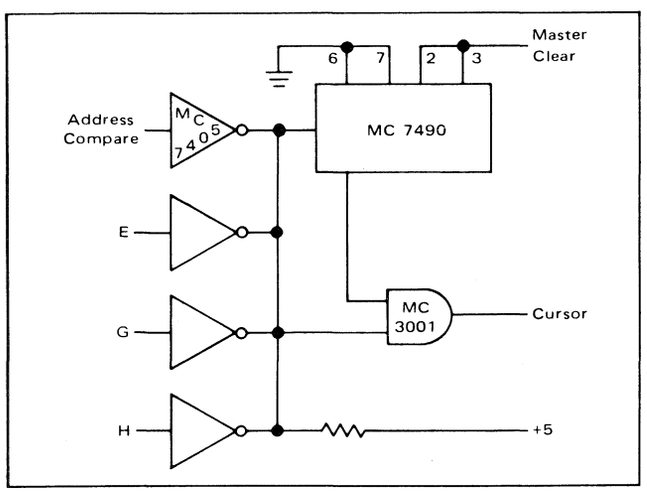


FIGURE 20

CONCLUSION

This system design shows one way of using the new NMOS devices in CRT systems for both storage and character generation. The simplicity of the design is possible because of the TTL compatibility and convenient power requirements of the NMOS parts. The capability of generating 128 characters in a 7 x 9 matrix and automatically shifting descender characters (g, j, p, q, and y) means a substantial reduction in external circuitry. The MC6545 Quad 80-bit Shift Register allows maximum design flexibility with features like a 3-state output, internal recirculate logic, a single clock input, and a frequency range of D.C. of 5 MHz. It will fit into small systems as a main storage device and into large systems as buffer storage. With these devices, NMOS has indeed arrived for the CRT display manufacturers.

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